DC Biasing of BJT

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Transistor Biasing

- A transistors steady state of operation depends a great deal on its base current, collector voltage, and collector current and therefore, if a transistor is to operate as a linear amplifier, it must be properly biased to have a suitable operating point.
- Transistor Biasing is the process of setting a transistors DC operating voltage or current conditions to the correct level so that any AC input signal can be amplified correctly by the transistor.

Transistor Biasing

- Establishing the correct operating point requires the proper selection of bias resistors and load resistors to provide the appropriate input current and collector voltage conditions.
- The correct biasing point for a bipolar transistor, either NPN or PNP, generally lies somewhere between the two extremes of operation with respect to it being either fully-ON or fully-OFF along its load line.
- This central operating point is called the Quiescent Operating Point, or **Q-point** for short.

Transistor Biasing

- Any increase in *ac* voltage, current, or power is the result of a transfer of energy from the applied *dc* supplies.
- The analysis or design of any electronic amplifier therefore has two components: a *dc* and an *ac* portion.
- Basic Relationships/formulas for a transistor:

$$V_{BE} \cong 0.7\ \text{V}$$

$$I_E = (\beta + 1)I_B \cong I_C$$

$$I_C = \beta I_B$$

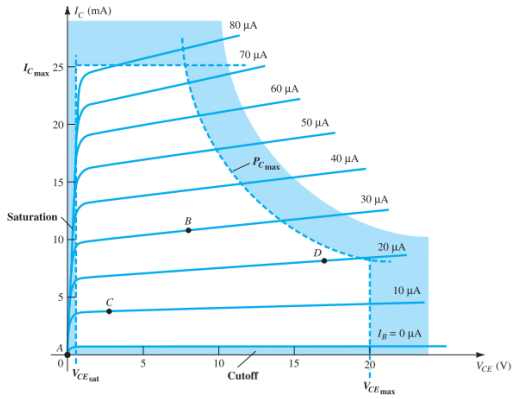
Operating Point

- For transistor amplifiers the resulting *dc* current and voltage establish an operating point on the characteristics that define the region that will be employed for amplification of the applied signal.
- Because the operating point is a fixed point on the characteristics, it is also called the quiescent point (abbreviated Q-point).

Operating Point

- Transistor Regions Operation:
  - Linear-region operation:
    - Base–emitter junction forward-biased
    - Base–collector junction reverse-biased
  - Cutoff-region operation:
    - Base–emitter junction reverse-biased
    - Base–collector junction reverse-biased
  - Saturation-region operation:
    - Base–emitter junction forward-biased
    - Base–collector junction forward-biased

Operating Point



Transistor Biasing

- Biasing is the process of providing DC voltage which helps in the functioning of the circuit.
- A transistor is based in order to make the emitter base junction forward biased and collector base junction reverse biased, so that it maintains in active region, to work as an amplifier.
- The proper flow of zero signal collector current, I_{CBO} and the maintenance of proper collector emitter voltage, V_{CE} during the passage of signal is known as **Transistor Biasing**. The circuit which provides transistor biasing is called as **Biasing Circuit**.

Need for DC biasing

- If a signal of very small voltage is given to the input of BJT, it cannot be amplified. Because, for a BJT, to amplify a signal, two conditions have to be met.
  - The input voltage should exceed **cut-in voltage** (i.e. more than 0.7 V) for the transistor to be **ON**.
  - The BJT should be in the **active region**, to be operated as an **amplifier**.

Need for DC biasing

- If appropriate DC voltages and currents are given through BJT by external sources, so that BJT operates in active region and superimpose the AC signals to be amplified, then this problem can be avoided.
- The given DC voltage and currents are so chosen that the transistor remains in active region for entire input AC cycle. Hence DC biasing is needed.
- For a transistor to be operated as a faithful amplifier, the operating point should be stabilized.

Factors Affecting The Q Point

- The main factor that affect the operating point is the temperature. The operating point shifts due to change in temperature.
- As temperature increases, the values of I_{CE}, β, V_{BE} gets affected.
  - I_{CBO} gets doubled (for every 10^{o} rise)
  - V_{BE} decreases by 2.5mv (for every 1^{o} rise)
- Hence operating point should be made independent of the temperature so as to achieve stability. To achieve this, biasing circuits are introduced.

Bias Stabilization

- The process of making the operating point independent of temperature changes or variations in transistor parameters is known as **Bias Stabilization**.
- Once the bias stabilization is achieved, the values of I_C and V_{CE} become independent of temperature variations or replacement of transistor.
- A good biasing circuit helps in the bias stabilization of operating point.

Need for Bias Stabilization

- Stabilization of the operating point has to be achieved due to the following reasons.
  - Temperature dependence of I_C
  - Individual variations
  - Thermal runaway

Temperature Dependence of I_C

- As the expression for collector current I_C is

$$I_C = \beta I_B + I_{CEO}$$
$$I_C = \beta I_B + (1+\beta) I_{CBO}$$

- The collector leakage current I_{CBO} is greatly influenced by temperature variations.
- To come out of this, the biasing conditions are set so that zero signal collector current I_C = 1 mA.
- Therefore, the operating point needs to be stabilized i.e. it is necessary to keep I_C constant.

Individual Variations

- As the value of β and the value of V_{BE} are not same for every transistor, whenever a transistor is replaced, the operating point tends to change. Hence it is necessary to stabilize the operating point.

Thermal Runaway

- The flow of collector current and also the collector leakage current causes heat dissipation. If the operating point is not stabilized, there occurs a cumulative effect which increases this heat dissipation.
- The self-destruction of such an unstabilized transistor is known as **Thermal run away**.
- In order to avoid **thermal runaway** and the destruction of transistor, it is necessary to stabilize the operating point, i.e., to keep I_C constant.

Stability Factor

- The stability of a transistor is the ability to maintain the Q point along the load line.
- The extent to which the collector current I_C is stabilized with varying I_{CBO} is measured by a stability factor, *S*.
- It is defined as the rate of change of collector current I_C with respect to the collector base leakage current I_{CBO} or I_{CO}, keeping both the current I_B and the current gain β constant.

$$S = \left.\frac{dI_C}{dI_{CO}}\right|_{I_B,\beta}$$

Stability Factor

- Hence we can understand that any change in collector leakage current changes the collector current to a great extent.
- The stability factor should be as low as possible so that the collector current doesn't get affected. S = 1 is the ideal value.
- The general expression of stability factor for a CE configuration can be obtained as under.

$$I_C = \beta I_B + (1+\beta) I_{CBO}$$

- or $$I_C = \beta I_B + (1+\beta) I_{CO}$$

Stability Factor

- Differentiating above expression with respect to I_C, we get

$$1 = \beta \frac{dI_B}{dI_C} + (1+\beta)\frac{dI_{CO}}{dI_C}$$

$$1 = \beta \frac{dI_B}{dI_C} + (1+\beta)\frac{1}{S}$$

- Hence, Stability Factor $$S = \frac{(1+\beta)}{\left(1-\beta\left(\frac{dI_B}{dI_C}\right)\right)}$$

- Hence the stability factor S depends on β, I_B and I_C.

Transistor DC Bias Configurations

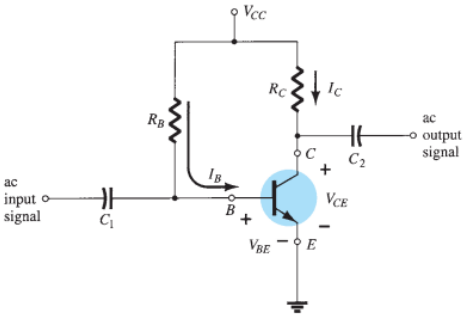
- Biasing means applying of *dc* voltages to establish a fixed level of current and voltage >>> Q-Point.
  - Fixed-Bias Configuration
  - Emitter-Bias Configuration
  - Voltage-Divider Bias Configuration
  - Collector Feedback Configuration
  - Emitter-Follower Configuration
  - Common-Base Configuration
  - Miscellaneous Bias Configurations

Fixed-Bias Configuration

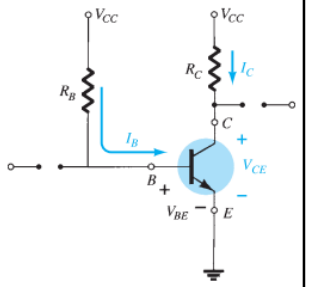
- The fixed-bias circuit provides a relatively straightforward and simple introduction to transistor *dc* bias analysis.
- Even though the network employs an *npn* transistor, the equations and calculations apply equally well to a *pnp* transistor configuration merely by changing all current directions and voltage polarities.
- For the *dc* analysis the network can be isolated from the indicated *ac* levels by replacing the capacitors with an open circuit equivalent.
- In addition, the dc supply V_{CC} can be separated into two supplies to permit a separation of input and output circuits.

Fixed-Bias Configuration

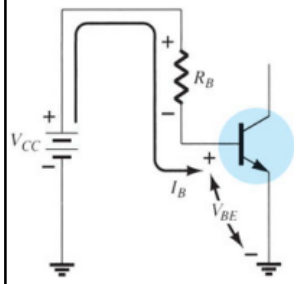
Fixed-bias circuit



DC equivalent circuit



Fixed-Bias Configuration



- **Base – Emitter loop:** Writing KVL equation in the clockwise direction for the loop, we obtain

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

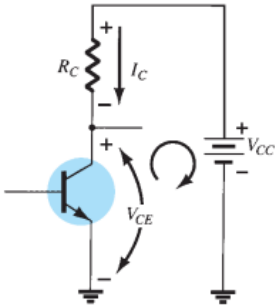
- Solving the equation for the current I_B will result in the following:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Fixed-Bias Configuration

- The base current is the current through R_B and by Ohm's law that current is the voltage across R_B divided by the resistance R_B.
- The voltage across R_B is the applied voltage V_{CC} at one end less the drop across the base-to-emitter junction (V_{BE}).
- In addition, since the supply voltage V_{CC} and the base–emitter voltage V_{BE} are constants, the selection of a base resistor, R_B, sets the level of base current for the operating point.

Fixed-Bias Configuration



- **Collector – Emitter loop:** The magnitude of the collector current is related directly to I_B through

$$I_C = \beta I_B$$

Applying KVL in the clockwise direction around the indicated closed loop will result in the following:

$$V_{CE} + I_C R_C - V_{CC} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$

Fixed-Bias Configuration

- which states in words that the voltage across the collector–emitter region of a transistor in the fixed-bias configuration is the supply voltage less the drop across R_C.
- As a brief review of single- and double-subscript notation recall that

$$V_{CE} = V_C - V_E$$

- where V_{CE} is the voltage from collector to emitter and V_C and V_E are the voltages from collector and emitter to ground, respectively.

Fixed-Bias Configuration

- But *in this case, since* $V_E = 0$ V, we have

$$V_{CE} = V_C$$

- In addition, since

$$V_{BE} = V_B - V_E$$

- and $V_E = 0$ V, then

$$V_{BE} = V_B$$

Stability Factor - FB

- As we know, $I_C = \beta I_B + (1+\beta) I_{CO}$
- and

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

- Substituting I_B into the equation of collector current I_C,

$$I_C = \beta \frac{V_{CC} - V_{BE}}{R_B} + (1+\beta) I_{CO}$$

- Differentiating wrt I_C,

$$1 = 0 + (1+\beta) \frac{dI_{CO}}{dI_C}$$

Stability Factor - FB

- The Stability factor,

$$S = \frac{dI_C}{dI_{CO}} = 1 + \beta$$

- Thus, the stability factor in a fixed bias is (1 + β) which means that I_C changes (1 + β) times as much as any change in I_{CO}.

Fixed-Bias Configuration

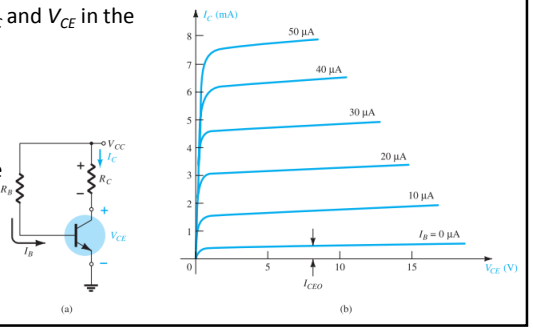
(a) The network, (b) The device characteristics

Load Line Analysis:

The network establishes an output equation that relates the variables I_C and V_{CE} in the following manner:

$$V_{CE} = V_{CC} - I_C R_C$$

The output characteristics of the transistor also relate the same two variables I_C and V_{CE}.



Fixed-Bias Configuration

- We have a network equation and a set of characteristics that employ the same variables.
- The common solution of the two occurs where the constraints established by each are satisfied simultaneously.
- In other words, this is similar to finding the solution of two simultaneous equations: one established by the network and the other by the device characteristics.
- We must now superimpose the straight line defined by network equation on the characteristics.
- The most direct method of plotting equation on the output characteristics is to use the fact that a straight line is defined by two points.

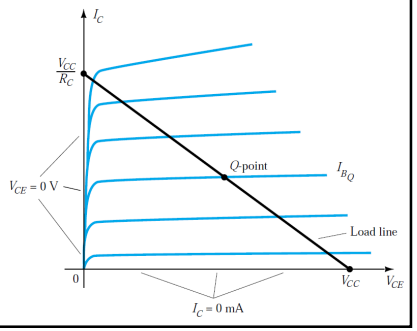
Fixed-Bias Configuration

Fixed-bias load line.

- If we choose I_C to be 0 *mA*, we are specifying the horizontal axis as the line on which one point is located.
- By substituting I_C = 0 *mA*, we find that

$$V_{CE} = V_{CC} - (0)R_C$$

$$V_{CE} = V_{CC}|_{I_C = 0\text{ mA}}$$



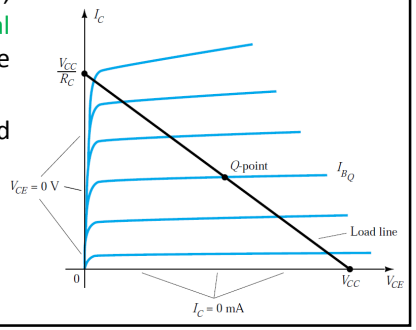
Fixed-Bias Configuration

Fixed-bias load line.

- If we now *choose* V_{CE} to be 0 V, which establishes the vertical axis as the line on which the second point will be defined
- We find that I_C is determined by the following equation:

$$0 = V_{CC} - I_C R_C$$

$$I_C = \frac{V_{CC}}{R_C}\bigg|_{V_{CE}=0\text{ V}}$$



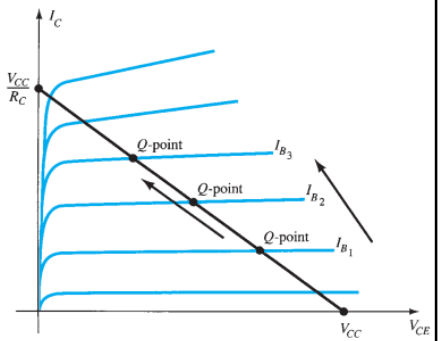
Fixed-Bias Configuration

- By joining the two points defined by two equations, the straight line established by network equation can be drawn. The resulting line on the graph is called the *load line* since it is defined by the load resistor R_C.
- By solving for the resulting level of I_B, the actual Q-point can be established.

Fixed-Bias Configuration

Movement of Q-point with increasing level of I_B.

If the level of I_B is changed by varying the value of R_B the *Q-point* moves up or down the load line

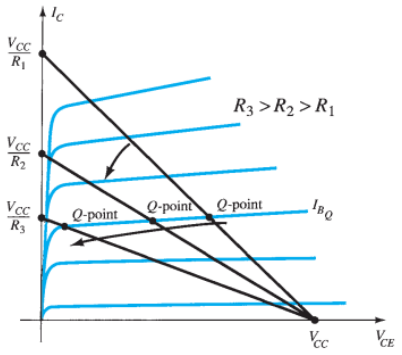


Fixed-Bias Configuration

Effect of increasing levels of R_C on the load line and *Q*-point.

If V_{CC} is held fixed and R_C changed, the load line will tilt vertically.

If I_B is held fixed, the *Q-point* will move downward, if R_C increases and vice-versa.

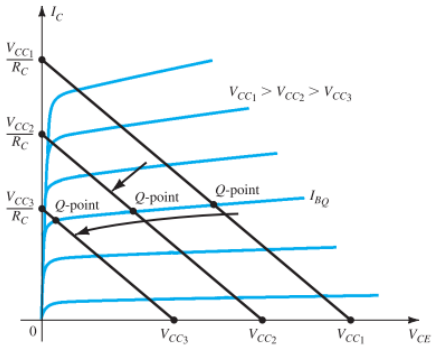


Fixed-Bias Configuration

Effect of lower values of V_{CC} on the load line and *Q*-point.

If R_C is fixed and V_{CC} varied, the load line will shift horizontally.

If I_B is held fixed, the *Q-point* will move downward, if V_{CC} decreases and vice-versa.



Fixed-Bias Configuration

- The dc bias network contains an emitter resistor to improve the stability level over that of the fixed-bias configuration.
- The addition of the emitter resistor to the dc bias of the BJT provides improved stability, i.e., the dc bias currents and voltages remain closer to where they were set by the circuit when outside conditions, such as temperature, and transistor beta, change.
- The analysis will be performed by first examining the base–emitter loop and then using the results to investigate the collector–emitter loop.

Fixed-Bias Configuration

Advantages

- The circuit is simple.
- Only one resistor R_B is required.
- Biasing conditions are set easily.
- No loading effect as no resistor is present at base-emitter junction.

Fixed-Bias Configuration

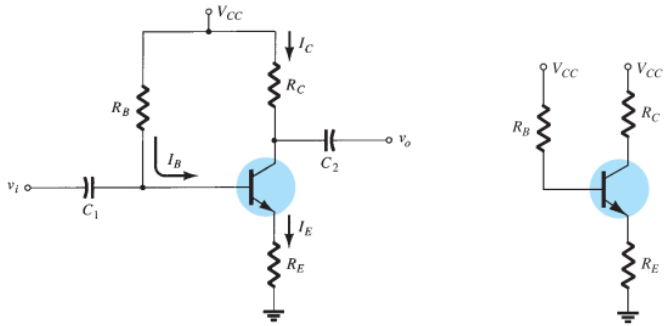
Disadvantages

- The stabilization is poor as heat dissipation can't be stopped.
- The stability factor is very high.
- So, there are strong chances of thermal runaway.

Hence, this method is rarely employed.

Emitter-Bias Configuration

BJT bias circuit with emitter resistor **DC equivalent circuit**



Emitter-Bias Configuration

Base-Emitter Loop

- Writing KVL around the base-emitter loop

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

- As we know,

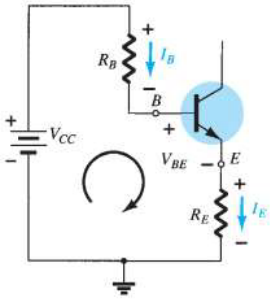
$$I_E = I_C + I_B$$

- Thus,

$$V_{CC} - I_B(R_B + R_E) - V_{BE} - I_C R_E = 0$$

- Hence the base current, I_B

$$I_B = \frac{V_{CC} - V_{BE} - I_C R_E}{(R_B + R_E)}$$



Emitter-Bias Configuration

Collector-Emitter Loop

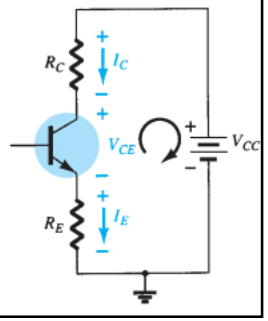
- Writing KVL for the indicated loop in the clockwise direction will result in

$$+I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

- Substituting, $I_E \cong I_C$

$$\boxed{V_{CE} = V_{CC} - I_C(R_C + R_E)}$$

- R_E provides excellent stabilization in this circuit.



Stability Factor - EB

- As we know, $I_C = \beta I_B + (1+\beta) I_{CO}$
- and

$$I_B = \frac{V_{CC} - V_{BE} - I_C R_E}{(R_B + R_E)}$$

- Substituting I_B into the equation of collector current I_C,

$$I_C = \beta \left[\frac{V_{CC} - V_{BE} - I_C R_E}{(R_B + R_E)}\right] + (1+\beta) I_{CO}$$

- Differentiating wrt I_C,

$$1 = \frac{\beta}{(R_B + R_E)}[0 - 0 - R_E] + (1+\beta)\frac{dI_{CO}}{dI_C}$$

Stability Factor -EB

- and

$$1 = -\frac{\beta R_E}{(R_B + R_E)} + (1+\beta)\frac{dI_{CO}}{dI_C}$$

$$S = \frac{(1+\beta)}{1 + \frac{\beta R_E}{(R_B + R_E)}}$$

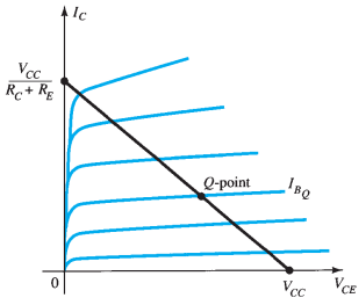
- The Stability factor,

$$S = \frac{dI_C}{dI_{CO}} = \frac{(1+\beta)(R_B + R_E)}{R_B + (1+\beta)R_E}$$

Emitter-Bias Configuration

Load-line Analysis

- The load-line analysis of the emitter-bias network is only slightly different from that encountered for the fixed-bias configuration.
- The level of I_B as determined defines the level of I_B on the characteristics as I_{BQ}.



Emitter-Bias Configuration

- The collector–emitter loop equation that defines the load line is the following:

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

- Choosing $I_C = 0$ mA gives

$$V_{CE} = V_{CC}\big|_{I_C = 0\text{ mA}}$$

- Choosing $V_{CE} = 0$ V gives

$$I_C = \frac{V_{CC}}{R_C + R_E}\bigg|_{V_{CE} = 0\text{ V}}$$

- Different levels of I_{BQ} will, of course, move the Q-point up or down the load line.

Emitter-Bias Configuration

Advantages

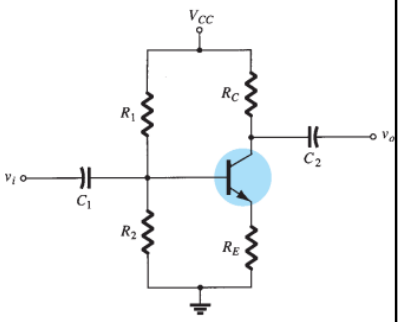
- The circuit is simple as it needs only two resistor.
- This circuit provides good stabilization, for lesser changes.
- When collector current rises, the emitter current will also increase resulting in an increased voltage drop across the emitter and hence the base current decreases considerably, ultimately leading to a reduction in the collector current thus stabilizing it for the temperature effect. This ensures that the operating point of the transistor is well within the specified region and also prevents thermal runaway.

Disadvantages

- The circuit doesn't provide good biasing.
- It reduces the gain of the amplifier considerably.

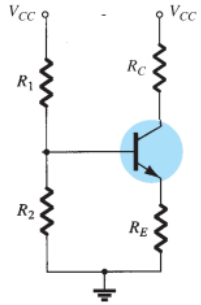
Voltage Divider-Bias Configuration

- Among all the methods of providing biasing and stabilization, the **voltage divider bias method** is the most prominent one.
- Here, two resistors R_1 and R_2 are employed, which are connected to V_{CC} and provide biasing.
- The resistor R_E employed in the emitter provides stabilization.



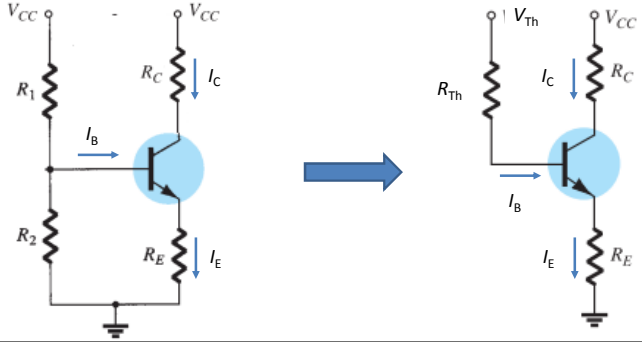
Voltage Divider-Bias Configuration

- The name voltage divider comes from the voltage divider formed by R_1 and R_2.
- The voltage drop across R_2 forward biases the base-emitter junction.
- This causes the base current and hence collector current flow in the zero signal conditions.



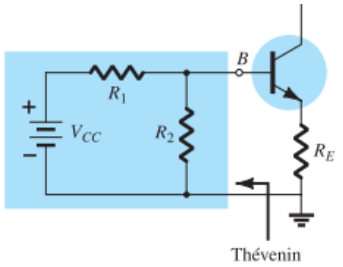
Voltage Divider-Bias Configuration

- Convert Voltage Divider to Emitter-Bias Configuration



Voltage Divider-Bias Configuration

- The input side of the network of voltage divider can be redrawn as shown in Figure for the dc analysis.
- The Thévenin equivalent network for the network to the left of the base terminal can then be found in the following manner:

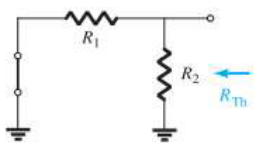


Voltage Divider-Bias Configuration

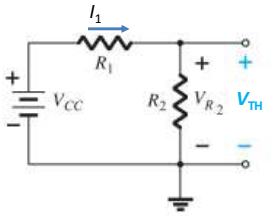
R_{Th}: The voltage source is replaced by a short-circuit equivalent as shown in Figure.

$$R_{TH} = R_1 \| R_2$$

$$R_{TH} = \frac{R_1 R_2}{(R_1 + R_2)}$$



V_{Th}: The voltage source V_{CC} is returned to the network and the open-circuit Thévenin voltage determined as follows:



Voltage Divider-Bias Configuration

- Applying the voltage-divider rule,

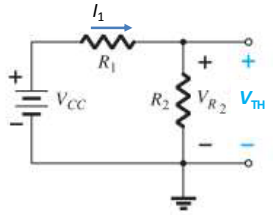
$$V_{CC} - I_1(R_1 + R_2) = 0$$

- Therefore, current flowing through Voltage Divider circuit,

$$I_1 = \frac{V_{CC}}{(R_1 + R_2)}$$

- and the voltage across equivalent resistance R_{TH} is

$$V_{TH} = V_{R_2} = \left[\frac{V_{CC}}{(R_1 + R_2)}\right] R_2$$



Voltage Divider-Bias Configuration

Base-Emitter Loop

- Writing KVL around the base-emitter loop

$$V_{Th} - I_B R_B - V_{BE} - I_E R_E = 0$$

- As we know,

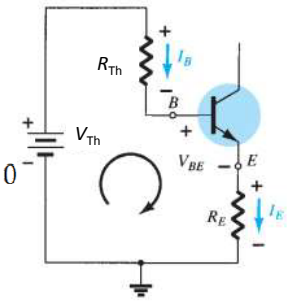
$$I_E = I_C + I_B$$

- Thus,

$$V_{Th} - I_C(R_{Th} + R_E) - V_{BE} - I_E R_E = 0$$

- Hence the base current, I_B

$$I_B = \frac{V_{Th} - V_{BE} - I_C R_E}{R_{TH} + R_E}$$



Voltage Divider-Bias Configuration

Collector-Emitter Loop

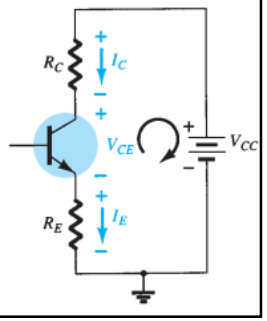
- Writing KVL for the indicated loop in the clockwise direction will result in

$$+I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

- Substituting, $I_E \cong I_C$

$$\boxed{V_{CE} = V_{CC} - I_C(R_C + R_E)}$$

- R_E provides excellent stabilization in this circuit.



Stability Factor - VD

- As we know, $I_C = \beta I_B + (1+\beta) I_{CO}$
- and $I_B = \dfrac{V_{Th} - V_{BE} - I_C R_E}{R_{TH} + R_E}$
- Substituting I_B into the equation of collector current I_C,

$$I_C = \beta \left[\frac{V_{TH} - V_{BE} - I_C R_E}{(R_{TH} + R_E)} \right] + (1+\beta) I_{CO}$$

- Differentiating *wrt* I_C,

$$1 = \frac{\beta}{(R_{TH} + R_E)} [0 - 0 - R_E] + (1+\beta) \frac{dI_{CO}}{dI_C}$$

Stability Factor - VD

- and $$1 = \frac{\beta R_E}{(R_{TH} + R_E)} + (1+\beta) \frac{dI_{CO}}{dI_C}$$

$$S = \frac{(1+\beta)}{1 + \dfrac{\beta R_E}{(R_{TH} + R_E)}}$$

- The Stability factor,

$$S = \frac{dI_C}{dI_{CO}} = \frac{(1+\beta)(R_{TH} + R_E)}{R_{TH} + (1+\beta) R_E}$$

Stability Factor - VD

- If the ratio R_{TH}/R_E is very small, then R_{TH}/R_E can be neglected as compared to 1 and the stability factor becomes,

$$S = (1+\beta) \frac{\left(\dfrac{R_{TH}}{R_E} + 1 \right)}{\left(\dfrac{R_{TH}}{R_E} + (1+\beta) \right)}$$

$$S \cong \frac{(1+\beta)}{(1+\beta)} = 1$$

- This is the smallest possible value of S and leads to the maximum possible thermal stability.

Voltage Divider-Bias Configuration

Advantage

- Voltage divider bias circuit can successfully provide a d.c. Bias which is independent of the transistor current gain (β).
- This bias circuit has the smallest possible value of stability factor S and leads to the maximum possible thermal stability.
- Due to design considerations, R_{TH}/R_E has a value that cannot be neglected as compared to 1. In actual practice, the circuit may have stability factor around 10.

Voltage Divider-Bias Configuration

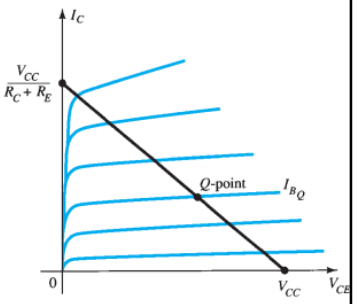
Disadvantages

- Requires more components than most of the other biasing circuits.

Voltage Divider-Bias Configuration

Load-Line Analysis

- The similarities with the output circuit of the emitter-biased configuration result in the same intersections for the load line of the voltage-divider configuration.
- The load line will therefore have the same appearance as that of emitter-biased circuit. Hence,



Voltage Divider-Bias Configuration

- The collector–emitter loop equation that defines the load line is the following:

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

- Choosing $I_C = 0$ mA gives

$$V_{CE} = V_{CC}\big|_{I_C = 0\text{ mA}}$$

- Choosing $V_{CE} = 0$ V gives

$$I_C = \frac{V_{CC}}{R_C + R_E}\bigg|_{V_{CE} = 0\text{ V}}$$

- The level of I_B is determined by a different equation for the voltage-divider bias and the emitter-bias configuration.

DC Biasing of BJT

END